No. LCY-95099

SHARP CORPORATION

TECHNICAL LITERATURE

FOR

TFT-LCD module

MODEL NO. LQ5AW01

DATE Oct. 5. 1995

The technical literature is subject to change without notice. So, please contact SHARP or its agency to start workings for mass production

SHARP CORPORATION

LIQUID CRYSTAL DISPLAY GROUP

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CONTENTS

The contents of this specification is target for mass produced module.

A trial product is the case of dissatisfied contents.

(1)Introduction

The SHARP Color TFT-LCD module is an active matrix LCD (Liquid Crystal Display) produced by making the most of Sharp's expertise in liquid-crystal and semiconductor technologies. The active device is amorphous silicon TFT (Thin Film Transistor). The module accepts full color video signal conforming to the NTSC(M) and PAL(B·G) system standards.
It can withstand an intense environment, the outline dimension is suitable for an auto-mobile display, compact size, compatible with 2DIN size.

(2)Features

- Dual mode type. [NTSC(M) and PAL(B·G) standards]
- MBK-PAL, or MaBiKi("thinning" in Japanese)-PAL which enables the 234-scanning lines panel to display a picture with virtually 273-scanning lines.
- TFT-active matrix-LCD drive system with high-contrast.
- 74,880 pixels (RGB Stripe configuration and full color) 5" diagonal size.
- Slim, lightweight and compact

①Active area/Outline area= 70% ②Thickness:16. 5mm ③Mass : ( ) g

- Built-in video interface circuit and 'control circuit responsive to two sets of standard R·G·B analog video signals.

"Reduced reflection as a result of low reflectance Black-Matrix and Anti-Gradation polarizer being adopted.

- It is possible to use both the same and the independent time sampling.
- An external clock mode is available.
- Optical viewing angle : 6 o'clock direction.

(Customers can use this module as a '12 o'clock viewing direction type' by using a display rotating function to rotate right/left and up/down scanning direction electrically.)

- This module includes a high luminance edge light that is excellent at low temperature.
- It is possible to use the dimming frequency(PWM) for back light.

(3)Construction and Outline

.Outline dimensions of TFT-LCD module: See Fig. 1

.The module consists of a TFT-LCD panel, driver ICS, control PWB mounted with electronic circuits, edge light, frame, front and rear shielding cases.
(Backlight driving DC/AC inverter is not built in the module.)

(4) Module geometry (Mechanical specification)

Tabel 1

Parameter	Specification	Unit	Remarks
Display format	74,880 960(H) × 234	Pixels\ dots	
Active area	102. 7(H)x 74.9 (V)	mm	
Screen size (Diagonal)	13 [5" 1	cm	
Dot pitch	0.107(H)X0.32 O(V)	mm	
Dot configuration	R·G·B Stripe configuration		
Outline dimension	126. 8(W) X89. 6(H) X16.5(D)	mm	[Note 4-1]
Mass	( )	g	

[Note 4－1]This measurement is typical, and in detail, see figure of outline .

(5)Input/output terminals and their descriptions

5-1)TFT-LCD panel driving section

Table 2 (Hi means VSH, Lo means GND.)

Pin No.	Symbol	i / o	Description	Remarks
1	HSY	i , o	Input/output horizontal sync. signal (low active)	[Note 5-1]
2	VSY	i , o	Input/output vertical sync. signal (low active)	[Note 5-2]
3	PWM	o	Terminal for output PWM of dimming back light.	[Note 5-3]
4	NTP	i	Terminal for display mode change of NTSC and PAL	[Note 5-4]
5	HRV	i	Turning the direction of horizontal scanning	[Note 5-5]
6	VRV	i	Turning the direction of vertical scanning	[Note 5-61
7	VSW	i	Selection signal of two sets of video signals	[Note 5-7]
8	SAM	i	Terminal for sampling mode change	[Note 5-8]
9	V_{CDC}	i	DC bias voltage adjusting terminal of common electrode driving signal	[Note 5-9]
10	VSH	i	Positive power supply voltage	
11	VBS	i	Composite video signal for sync. separator	[Note 5-101
12	BRT	i	Brightness adjusting terminal	[Note 5-111
13	VR1	i	Color video signal (Red) 1	Positive (On when VSW=Hi.)
14	VG1	i	Color video signal (Green) 1	Ditto
15	VB1	i	Color video signal (Blue) 1	Ditto
16	VSL	i	Negative power supply voltage	
17	VR2	i	Color video signal (Red) 2	Positive (On when VSW=Lo.)
18	VG2	i	Color video signal (Green) 2	Ditto
19	VB2	i	Color video signal (Blue) 2	Ditto
20	GND	i	Ground	
21	CLKC	i	Change the input/output direction of CLK, HSY and VS'	[Note 5-121
22	CLK	i , o	Input/output clock signal	[Note 5-131

[Note 5-11 If CLKC=' Hi', this terminal outputs horizontal sync. signal in phase with VBS.
If CLKC=' LO', this terminal will be external horizontal sync. input terminal.

[Note 5-21 If CLKC=' Hi', this terminal outputs vertical sync. signal in phase with VBS.
If CLKC=' LO', this terminal will be external vertical sync. input terminal.

[Note 5-3] PWM signal is used for the PWM dimming frequency and it is easy to get PWM signal dimming by combining both HSY and PWM signal. But please use this PWM signal just in case of inputting standard NTSC or PAL signal.

[Note 5-4] This terminal is to switch display mode, and it is NTSC mode when NTP is 'High' and is PAL mode when NTP is 'Low'.

[Note 5-5] When this terminal is ' High' , it will be normal and when it is 'Low', it will display reversely on horizontal direction.

[Note 5-61 When this terminal is ' High', it will be normal and when it is 'Low', it will display reversely on vertical direction.

[Note 5-7] This terminal is to switch input for groups of R, G, B color video signals, and Input 1 (No. 13 to 15) is selected when VSW is ' High' and Input 2 (No. 17 to 19) is selected when VSW is 'Low'.

[Note 5-81 This terminal is to switch sampling mode. It is the different data-sampling timing at RGB dots when SAM is 'High' and it is the same data-sampling timing at RGB dots when SAM is 'Low'.

[Note 5-9] This terminal is applicable to the DC bias voltage adjusting terminal of common electrode driving signal. If power supply voltage is typical, it is not necessary to re-adjust it, so use it in the open condition.
However, in the case that power supply voltage is changed, or power supply voltage is reduced, please adjust it externally to get the best contrast with a resistor you add to this terminal, or semifixed resistor, VCDC, in module. A recommended circuit is shown in Fig. 5.

[Note 5-10] The sync. signal which will be input, is negative polarity, and is applicable to standard composite sync. signal, negative one, in the same pulse level.

[Note 5-11] DC voltage supplied charged to this terminal. make the brightness of screen adjustable, that is, the black level of video signal adjustable.
Adjusting it in the time of delivery to get the best display in the condition of open terminal, you will be able to re-adjust it externally with a resistor you add to this terminal, or a semifixed resistor, BRT, in module. A recommended circuit is shown in Fig. 5.

[Note 5-121 CLKC='Hi' :CLK, HSY, VSY terminals are output mode.
CLKC=' LO' :CLK, HSY, VSY terminals are input mode.

[Note 5-13] If CLKC=' Hi', this terminal outputs 'Lo' voltage level.
If CLKC=' LO', this terminal will be external clock input terminal.

5-2) Functional reaching and Input/Output mode

Table 3

	CLKC="Hi"		CLKC="Lo"	
Terminal	SAM="Hi"	SAM="LO"	SAM="Hi"	SAM="LO"
HSY	output	output	Input	Input
VSY	output	output	Input	Input
CLK	Output "Lo voltage"	Output "Lo voltage"	Input "Dot clock"	Input "Pixel clock"

5-3)Backlight driving section

Table 4

terminals	No.	symbol	i/o	function	note
CN1	1	VL1	i	input terminal(hi voltage side)	[NOTE 5-14]
	2	NC	-1	non connection	
	3	VL2	-	input terminal(low voltage side)	
CN2	1	VL3	i	input terminal(hi voltage side)	
	2	NC	-	non connection	
	3	VL4	-	input terminal(low voltage side)	

[NOTE 5-14]1ow Voltage side of DC/AC inverter for backlight driving connects with Ground of inverter circuit.

(6) Absolute maximum ratings

Table 5 GND = 0V、Ta = 25℃

Parameter		Symbol	MIN	MAX	Unit	Remarks
Positive power supply voltage		V_{SH}	-0.3	+9.0	V	
Negative power supply voltage		V_{SL}	-6.0	+0.3	V	
Analog input signals		Vi	—	2.0	V p-p	[Note 6-1]
Digital input/output signals		VI	-0.3	+5.4	V	[Note 6-21
DC bias voltage of common electrode driving signal		V_{CDC}	V_{SL}	V_{SH}	V	
Brightness adjusting terminal		V_{BRT}	0	+5.1	V	
Storage temperature		T stg	-30	85	℃	[Note 6-31
Operating temperature	surface of panel	Top1	-30	85	℃	[Note 6-3,4'
	environment	T_{OP2}	-30	60	℃	[Ditto]

[Note 6-11 VBS, VR1, VG1, VB1, VR2, VG2, VB2 terminals(Video signal)

[Note 6-2] NTP, HRV, VRV, SAM, VSW, HSY, VSY, CLKC, CLK terminals

[Note 6-3] The temperature of all parts in module should not be exceeding this rating.

Maximum wet-bulb temperature should less than 58℃. Do not dew condensation.

[Note 6-4] Operating temperature assure only driving .Contrast, response time,the other display quality is judgment at 25℃.

(7)Electrical characteristics

7-1) Recommended operating condition

A) TFT-LCD panel driving section

Table 6 GND = 0V, T_a = 25℃

Parameter		Symbol	MIN	TYP	MAX	Unit	Remarks
Positive power supply voltage		V_{SH}	+7.8	+8.0	+8.2	V	[Note 7-11
Negative power supply voltage		V_{SL}	-5.2	-5.0	-4.8	V	
Analog input voltage	Amplitude	VBS	0.7	1.0	2.0	Vp-p	Input resister
		V i l -		0.7 I -		Vp-p	【Note 7-2】 is over 10kΩ.
	DC component	V_{IDC}	−1.0	O	-1.0	V	[Note 7-3]
Digital input voltage	High level	V_{IH}	+3.7	-	+5.1	V	Input resister is over 10kΩ.
	Low level	V_{IL}	0	-	+1. O	V	【Note 7-41
	Hysteresis	V_H	0.4	-	-	V	
Digital output voltage	High level	V_{OH}	+4.0	-	-5.5	V	Load resister is over 60kΩ.
	Low level	V_{OL}	0	-	+1. o	V	【Note 7-51
Input horizontal sync. component	freq. NTSC	$f_{H(N)}$	15.13	15.73	16.33	kHz	CLKC="Hi"
	PAL	$f_{H(P)}$	15.03	15.63	16.23	kHz	【Note 7-61
	pulse NTSC	$\tau_{HI(N)}$	4.2	4.7	5.2	μs	for VBS terminal
	width PAL	$\tau_{HI(P)}$	4.2	4.7	5.2	μs	
	rise time	τ_{rHI1}	-	-	0.5	μs	
	fall time	τ_{fHI1}	-	-	0.5	μs	
Input vertical sync. component	freq. NTSC	$f_{V(N)}$	f_H/284	f_H/262	f_H/258	Hz	CLKC="Hi", H=1/f_H
	PAL	$f_{V(P)}$	f_H/344	f_H/312	f_H/304	Hz	[Note 7-7]
	pulse NTSC	$\tau_{VI(N)}$	-	3H	-	μs	for VBS terminal
	width PAL	$\tau_{VI(P)}$	-	2.5H	-	μs	
	rise time	τ_{rVI1}	-	-	0.5	μs	
	fall time	τ_{fVI1}	-	-	0.5	μs	
Input clock	frequency	fCL,	18.2	18.9	19.6	MHz	SAM="Hi" CLKC="LO"
		f_{CLI}	6.0	6.8	7.6	MHz	SAM="Lo" [Note 7-8]
	'Hi' width	τ_{WH}	20.0	-	-	ns	for CLK terminal
	'Lo' width	τ_{WL}	20.0	-	-	ns	
	rise time	τ_{rCLI}	-	-	5.0	ns	
	fall time	τ_{fCLI}	-	-	5.0	ns	
Input HSY Horizontal sync.)	frequency	f_{HI}	f_{CLI}/1230	f_{CLI}/1200	f_{CLI}/1170	Hz	SAM="Hi" CLKC="LO"
		f_{HI}	$f_{CL\ I}$/465	fCL [/435	f_{CLI}/405	Hz	SAM="Lo" [Note 7-91
	pulse width	τ_{HI}	1.0	4.7	8.4	μs	for HSY terminal
	rise time	$\tau_{rHI1\ 1}$	-	-	0.05	μs	
	fall time	τ_{fHI1}	-	-	0.05	μs	
Input VSY (Vertical sync.)	frequency	f_{VI}	50	f_{HI}/262	f_{HI}/258	Hz	[Note 7-10】CLKC="LO"
	pulse width	$\tau_{iV,\ (P)}$	1H	3H	5H	μs	for VSY terminal
	rise time	τ_{rVI2}		-	0.5	μs	
	fall time	τ_{fVI2}		-	0.5	us	
Data set up time		t_{SU1}	25	-	-	ns	[Note 7-11] CLKC="LO"
Data hold time		t_{HO1}	25	-	-	ns	
Data set up time		t_{SU2}	1.0	-	-	μs	【Note 7-12】
Data hold time		t_{HO2}	1.0	-	-	μs	
DC bias voltage for common electrode driving signal		V_{CDC}	+0.0	+1.5	+3.0	v	DC component [Note 7-13】
Terminal voltage applicable to brightness		V_{BRT}	+2.0	+2.3	+2.4	V	

[Note 7-1] Power supply voltage should not be changed after adjusting V_{CDC}.
[Note 7-21 VR1, VG1, VB1, VR2, VG2, VB2 terminals (Video signal)
[Note 7-3] VBS, VR1, VG1, VB1, VR2, VG2, VB2 terminals
[Note 7-41 HSY, VSY, NTP, VSW, HRV, VRV, SAM CLKC, CLK terminals
[Note 7-5] HSY, VSY, CLK terminals (output mode)
[Note 7-6] VBS (horizontal sync. component)
[Note 7-7] VBS (vertical sync. component)
[Note 7-81 CLK (input mode)
[Note 7-9] HSY (input mode)
[Note 7-101 VSY (input mode)
[Note 7-11] In case of CLKC=' Hi', it shows the phase difference from HSY to CLK. In that case, HSY will be taken at the rise timing of CLK.
[Note 7-12] In case of CLKC=' Hi', it shows the phase difference from VSY to HSY. In that case, VSY will be taken at the rise timing of HSY.
[Note 7-13] Adjusting the optimal voltage every module at the typical value of power supply voltage to get the maximum value of contrast. However, in the case that the power suPply voltage is changed, for example, the level of power supply voltage is reduced, please adjust it externally to get the best contrast with a resistor you add to this terminal, or semifixed resistor, VCDC, in module. A recommended circuit is shown in Fig. 3.

B)Backlight driving section

Table 7

Parameter	symbol	MIN	TYP	MAX	Unit	Remarks
lamp Voltage	VL_7	(280)	(320)	(360)	Vrms	I_L=7mArms
	VL_3	(380)	(430)	(480)	Vrms	I_L=7mArms
lamp current	I_L	3.0	-	7.5	mArms	
lamp frequency	f_L	20	-	70	KHz	
Kick-off voltage	V_s	-	-	650	Vrms	(Ta=+25℃)
				1000	Vrms	(Ta=-30℃)

7-2) Power consumption

Table 8 Ta=25°C

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Positive supply current	I_{SH}	$V_{SH}=+8.0V$	–	120	160	mA	
Negative supply current	I_{SL}	$V_{SL}=-5.0V$	–	40	55	mA	
Total	W_S		–	1.2	1.6	w	[Note 7-14]
lamp power consumption	W_L	normal driving		(4. 5)		w	[Note 7-15]

[Note 7-14] exclude backlight section

[Note 7-15 preference data by calculation ($I_L \times V_L \times 2$: number of lump)

7-3) Circuit diagram

The circuit block diagram of TFT-LCD module is shown in Fig. 2.

BRT, V_{CDC}, external adjusting recommended circuit is shown in Fig. 3.

Caution: Turn on or off the power supply (V_{SH} and V_{SL}) at the same time.
Be careful to supply all power voltage before inputting signals.

7-4) Input/output signal waveforms.

They are shown in Fig. 4.

Caution: For the VBS signal, input standard composite video (or sync.) signal applicable to the operating ❑ ode which have NTSC(M) or PAL(B·G) and is selected by the NTP signal.
A long time input of non-standard sync. signal may cause flicker or degradation of display quality.

7-5) Dimming backlight by PWM timing chart

In case of using PWM mode, please refer the timing chart shown in Fig. 5.

7-6) Input/Output signal timing chart

It is shown in fig. 4

Table 9 (CLKC="Hi"、NTSC: f_H=15.7kHz、f_V=60Hz／PAL: f_H=15.6kHz、f_V=50Hz)

Parameter		Symbol	MIN	TYP	MAX	Unit	Remarks
Horizontal sync. output pulse	pulse width	τ_{HS2}	2.9	3.9	4.9	μs	f=f_H [Note 7-20]
	phase difference	r pd	0.1	1.1	2.1	μs	[Note 7-21]
	rise time	τ_{rHO}	-	–	0.5	μs	C_L=10pF
	fall time	τ_{fHO}	-	–	0.5	μs	
Vertical sync. output pulse	pulse width	τ Vs	–	4H	-	μs	1H=1/f_H
	phase difference	τ_{VHO}	–	11.0	28.0	μs	[Note 7-22】
	rise time	τ_{rVO}	–	–	2.0	μs	C_L=10pF
	fall time	τ_{fVO}	–	–	2.0	μs	
Vertical phase difference	odd field	τ_{PV1}	-	1 H	-	μs	1H=1/f_H
	even field	τ_{PV2}	–	0.5H	-·	μs	[Note 7-23】

(Supply voltage condition: V_{SH}=+8.OV, V_{SL}=-5.OV)

[Note 7-20] Adjusted by variable resister (H-POS) in a module.

[Note 7-21] Variable range by variable resister (H-POS) in a module.

adjustment : τ pd = 1.1 ± 0.7 μs

[Note 7-22] Synchronized with HSY, basedon falling timing of HSY.

[Note 7-231 VSY signal delays.

7-7) Display time range

① NTSC(M) mode (NTP=' Hi', CLKC=' Hi')

Displaying the following range within video signals.

(a) Horizontally : 12.2 ~ 63.0 μs from the falling edge of HSY. (SAM=' Hi')

: 12.3 ~ 62.9 μs from the falling edge of HSY.(SAM=' LO')

(b) Vertically : 20 ~ 253 H from the falling edge of VSY.

② PAL(B·G) mode (NTP=' Lo', CLKC=' Hi')

Displaying the following range within video signals.

(a) Horizontally : 13.0 ~ 63.8 μs from the falling edge of HSY.(SAM=' Hi')

: 13.1 ~ 63.7 μs from the falling edge of HSY. (SAM=' Lo')

(b) Vertically : 26 ~ 298 H from the falling edge of VSY.

However, the video signals of (14n+12)H, (14n+20)H/Even field.

(14n+17)H, (14n+23)H/Odd field (n=1, 2·.● , 20)

are not displayed on the module.

③ External clock mode (NTP=' Hi', CLKC=' Lo')

Displaying the following range within video signals.

(a) Horizontally : 205 ~ 1164 clk from the falling edge of HSY.(SAM=' Hi')

: 84 ~ 403 clk from the falling edge of HSY.(SAM=' LO')

(elk means input external clock.)

(b) Vertically : 20 ~ 253 H from the falling edge of VSY.

(8)Optical characteristics

Table 10 Ta=25℃

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Viewing angel range		Δθ11	CR≥10	30	-	-	" (degree)	
		Δθ 12		10	-	-	" (degree)	
		Δθ 2		45	-	-	" (degree)	[Note 8-1.21
Contrast ratio		CRmax	Optimal	60	-	-		[Note 8-2,31
Response time	Rise	τr	θ=0°	-	30	60	ms	[Note 8-2,41
	Fall	rd			50	100	ms	
Luminance		Y	I_L=7mArms	-	(250)	-	cd/m²	[Note 8-51
	-30℃	Y_{Low}	I_L=7mArms	-	(30)	-	%	[Note 8-6,71
	adjustment lamp	Y_{DIM}	I_L=3mArms	-	( )	-	%	[Note 8-71
White chromaticity		x	IL=7mArms	0.263	0.313	0.363		[Note 8-51
		y	IL=7mArms	0.279	0.329	0.379		[Note 8-51
lamp life time	+25℃	-	continuation	10, 000	-	-	hour	[Note 8-81
	-30℃	"	intermission	2, 000	-	-	time	[Note 8-91

DC/AC inverter for external connection shown in following.

Harison Co. : HIU-275

[Note 8-1] Viewing angle range is defined as follows.

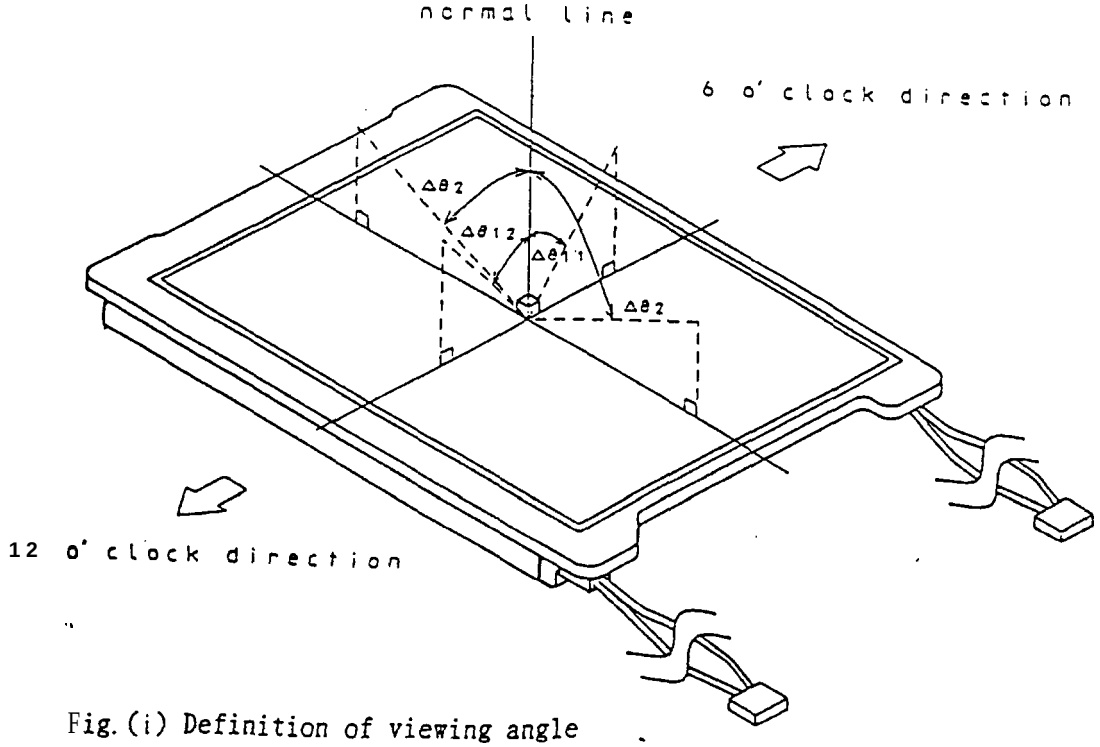


Fig. (i) Definition of viewing angle

[Note 8-21 Applied voltage condition:

"i) V_{CDC} is adjusted so as to attain maximum contrast ratio.

ii) Terminal adjustable to brightness (BRT) is open.

iii) Input video signal of standard black level and 100% white level.

[Note 8-31 Contrast ratio is defined as follows:

$$\text{Contrast ratio(CR)} = \frac{\text{Photodetector output with LCD being "white"}}{\text{Photodetector output with LCD being "black"}}$$

[Note 8-41 Response time is obtained by measuring the transition time of photodetector output, when input signals are applied so as to make the area "black" to and from "white".

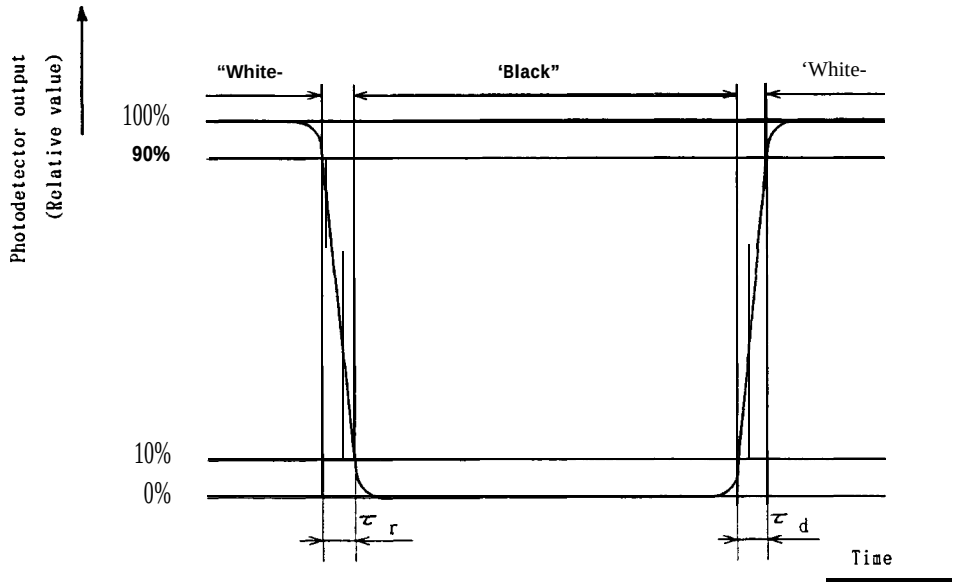


Fig. (ii)

[Note 8-5] Measuredon the center area of the panel at a viewing cone 1° by TOPCON luminance meter BM-7. (After 10 minutes operation)

DC/AC inverter driving frequency:43kHz

[Note 8-6] Ambient temperature: -30℃

Measured luminance on the panel after 5 minutes operation.

[Note 8-7] In case that the brightness is assumed 100% with following condition.

Ambient temperature:25℃

I_L=7mArms

after 10 minutes operation

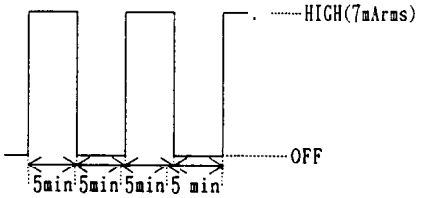
[Note 8-8] Lamp life time is defined as the time when either ① or ② occurs in the continuous operation under the condition of lamp current IL=3~7.5mArms and PWM dimming 100%~5%.(Ta=25℃)

①Brightness becomes 50% of the original value.

②Kick off voltage at Ta=-30℃ exceeds maxmumvalue, lOOOVrms.

[Note 8-9]The intermittent cycles is defined as a time when brightness becomes 50% of the original value under the condition of following cycle.

Ambient temperature: -30℃



(9)Mechanical characteristics

9-1) External appearance

Do not exist extreme defects. (See Fig. 1)

9-2) Panel toughness

The panel shall not be broken, when 19N is pressed on the center of the panel by a smooth sphere having 15 mm diameter.

Caution: In spite of very soft toughness, if, in the long-term, add pressure on the active area, it is possible to occur the functional damage.

9-3) Input/output connector performance

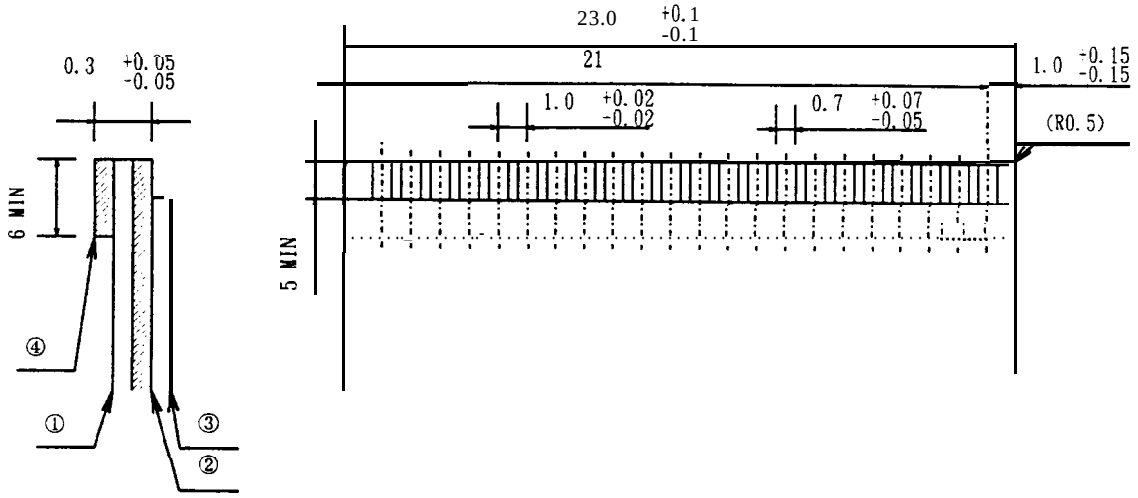
A)Input/output connectors for the operation of LCD module (FPC connector 22 pin)

inapplicable FPC Shown in Fig.(i).

ⅱ)Terminal holding force : More than 0.9N/pin

(Each terminal is pulled out at a rate of 25 ±3㎜/min.)

ⅲ)Insertion/pulling:contact resistance is not twice larger than the durability initial value after applicable FPC is inserted and pulled out 20 times



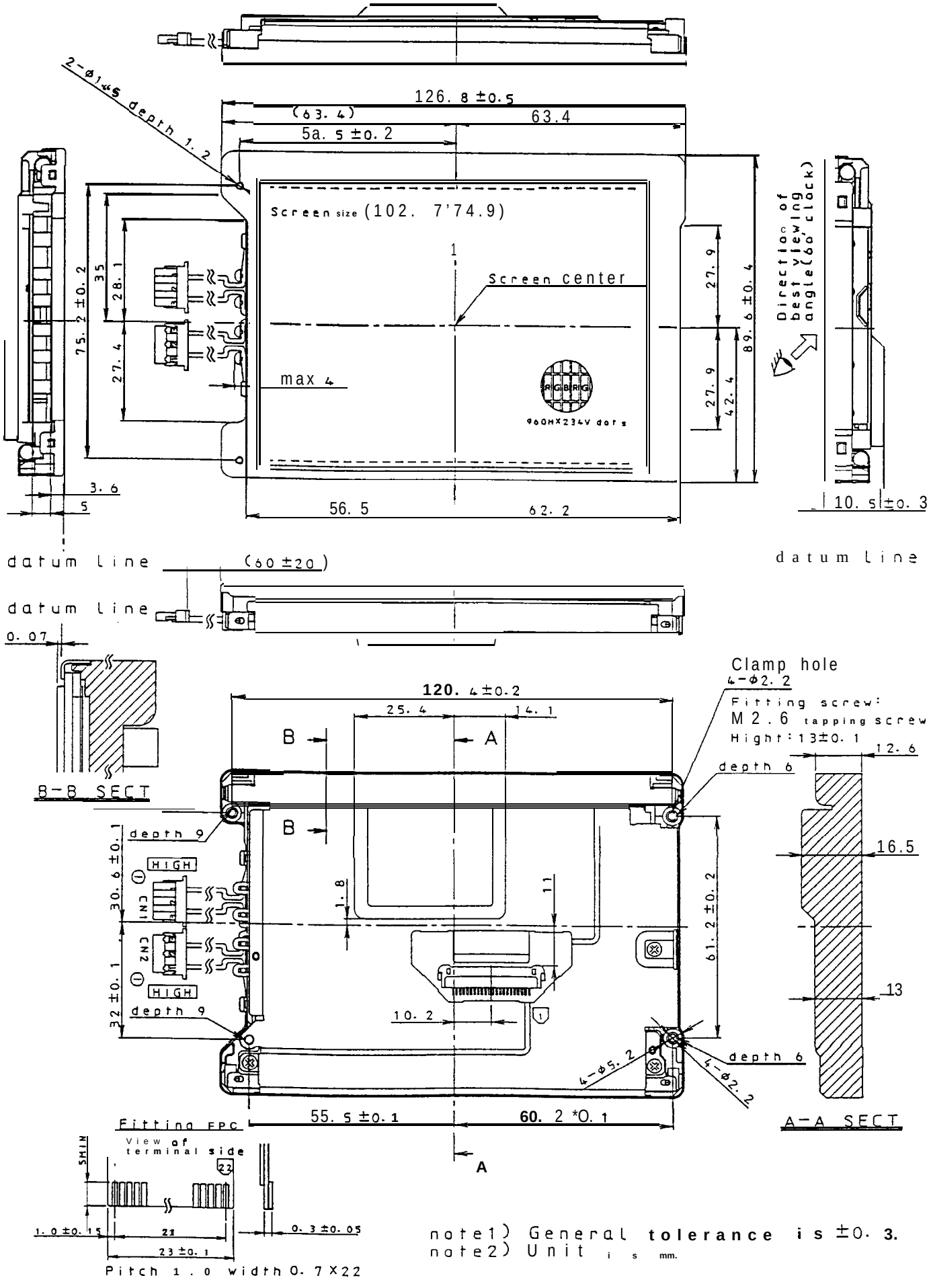
No.	N a m e	Materials
①	Base material	Polyimide or equivalent material(25㎛ thick)
②	Copper foil	Copper foil(35㎛ thick) Solder plated in 2 to 12㎛
③	Cover lay	Polyimide or equivalent material
④	Reinforcing plate	polyester polyimide or equivalent material(188㎛ thick)

Fig. (ⅲ) FPC applied to input/output connector (1.0㎜ pitch)

B)I/O connector of backlight driving circuit

Symbol	Used Connector	Corresponding connector	Manufacturer
CN1	BHR-03VS-1	SM02(8.O) B-BHS-TB(wire to board)	JST
		BHMR-03V(wire to wire)	JST
CN2	BHR-03VS-1	SM02(8.O) B-BHS-TB(wire to board)	JST
		BHMR-03V(wire to wire)	JST

Provisional specification
1995.



note1) General tolerance is ±0.3.
note2) Unit is mm.

Fig.1 Outline dimensions of TFT-LCD module

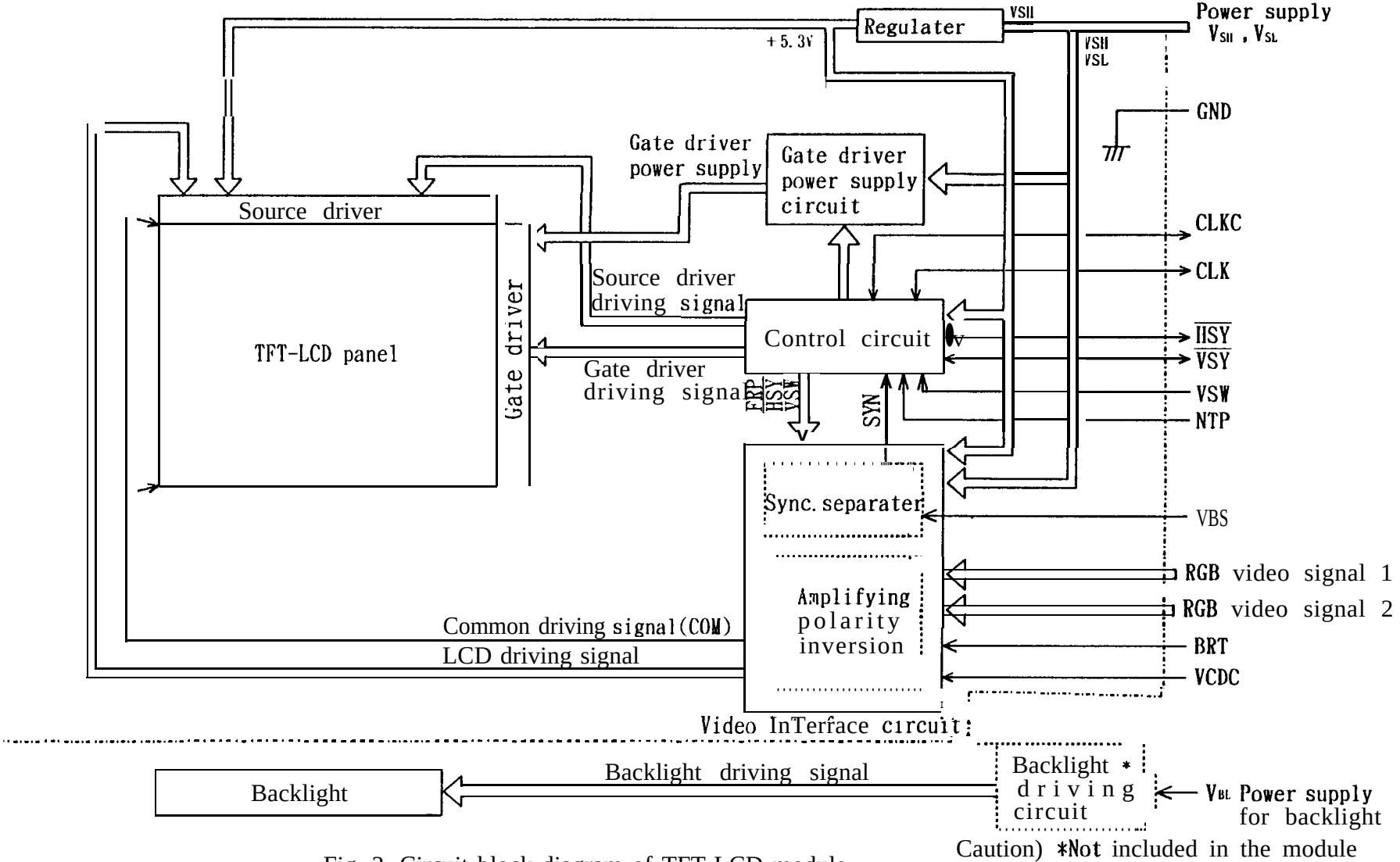
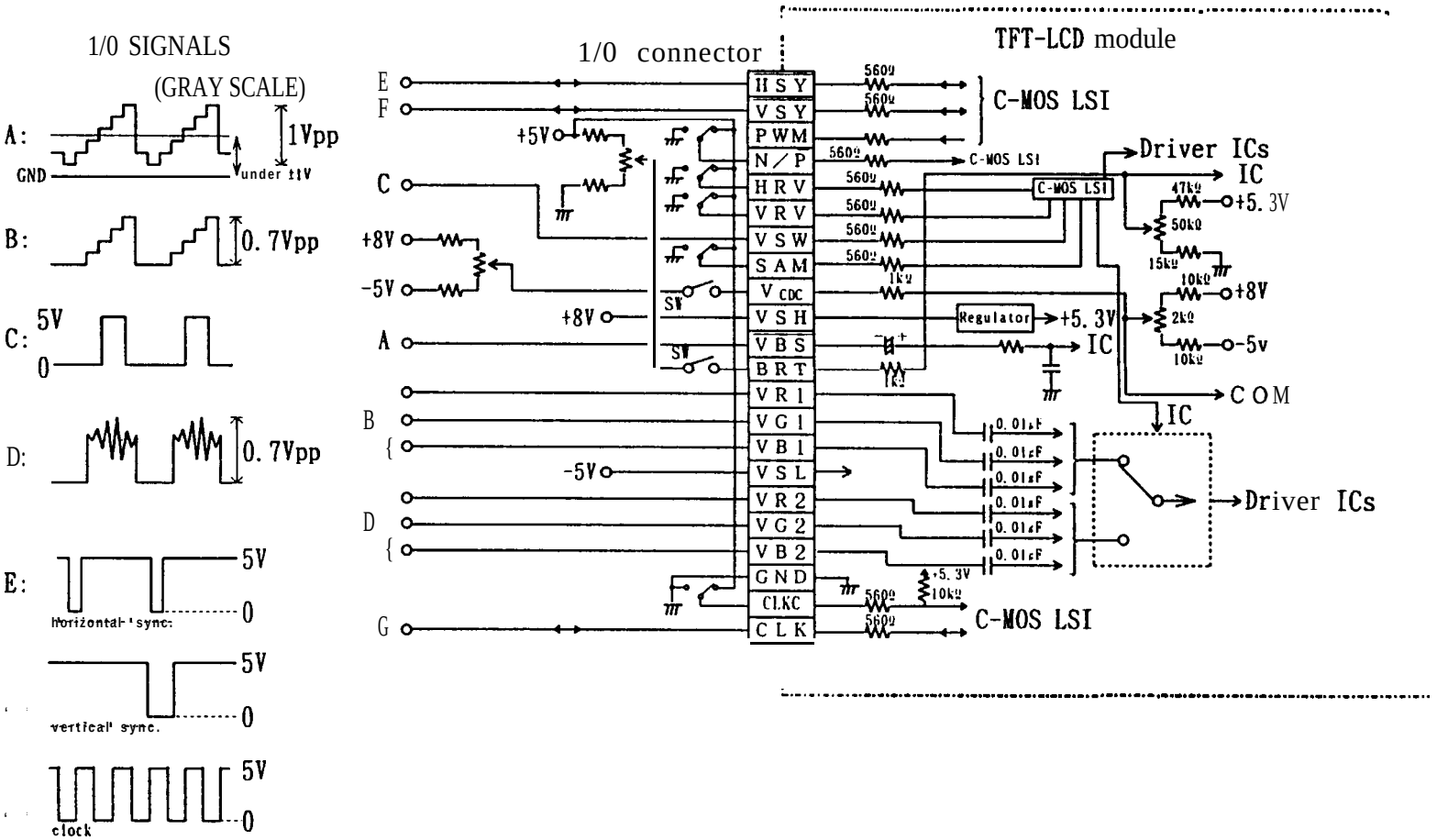


Fig. 2. Circuit block diagram of TFT-LCD module



(Note)
input impedance of A, B, D: >10kΩ
input impedance of C: >50kΩ

Fig. 3 Recommended circuit to refer

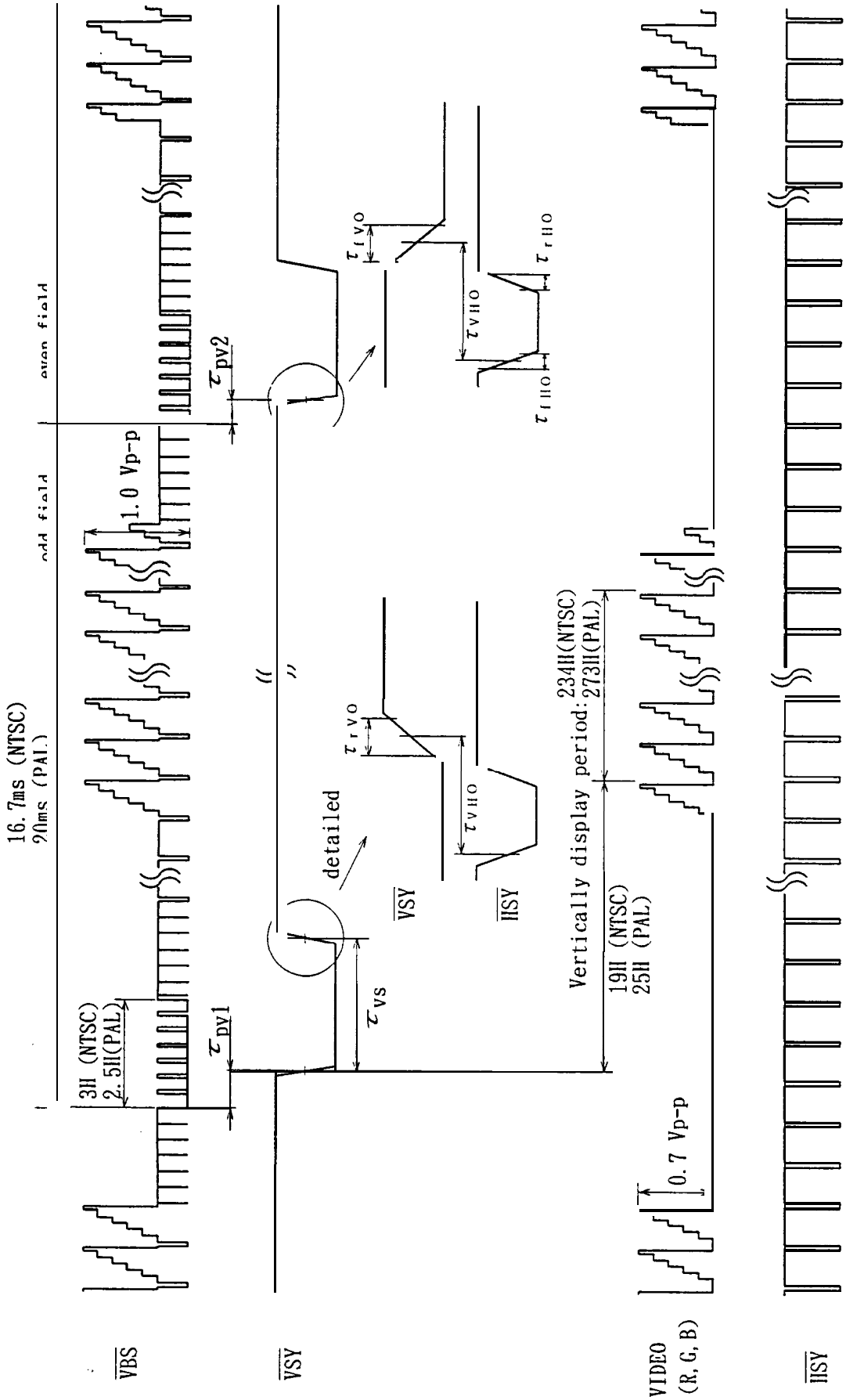


Fig. 4-A Input/Output signal waveforms(CLKC='Hi')

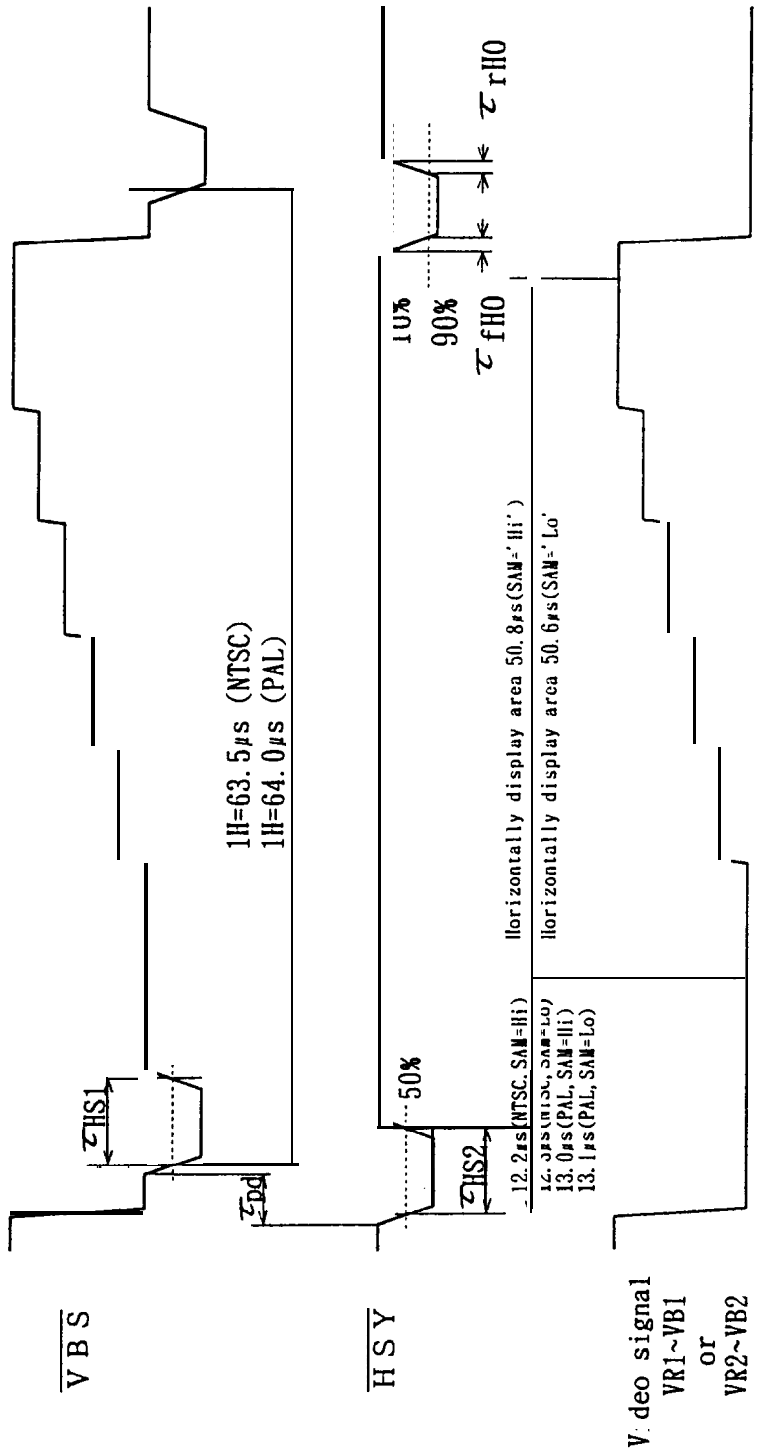


Fig.4-B nput/Output signal waveforms (CLKC='H')

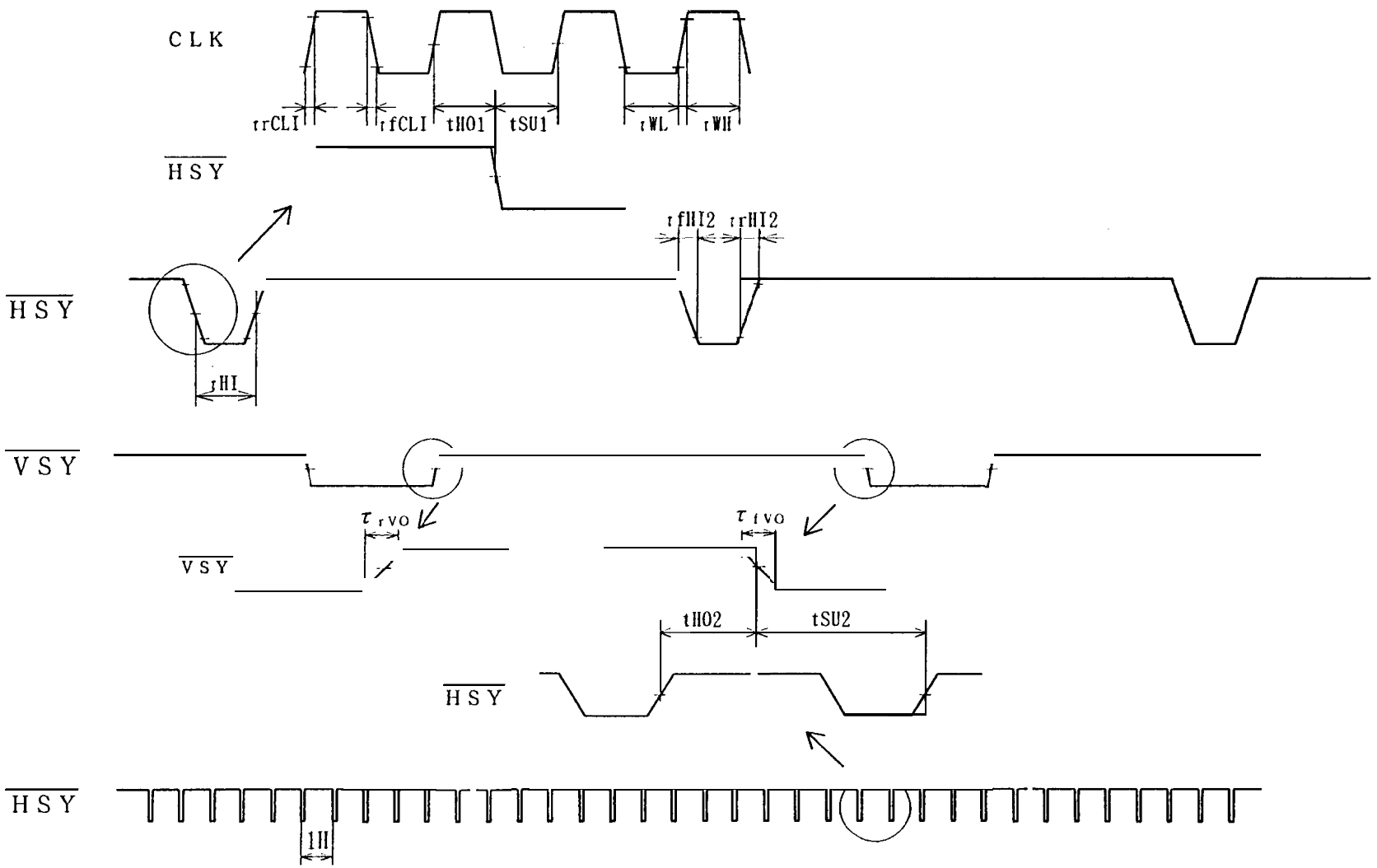


Fig. 4-C Inpu /Ou put s gnal waveforms(external clock mode NTP='H', CLKC='Lo')

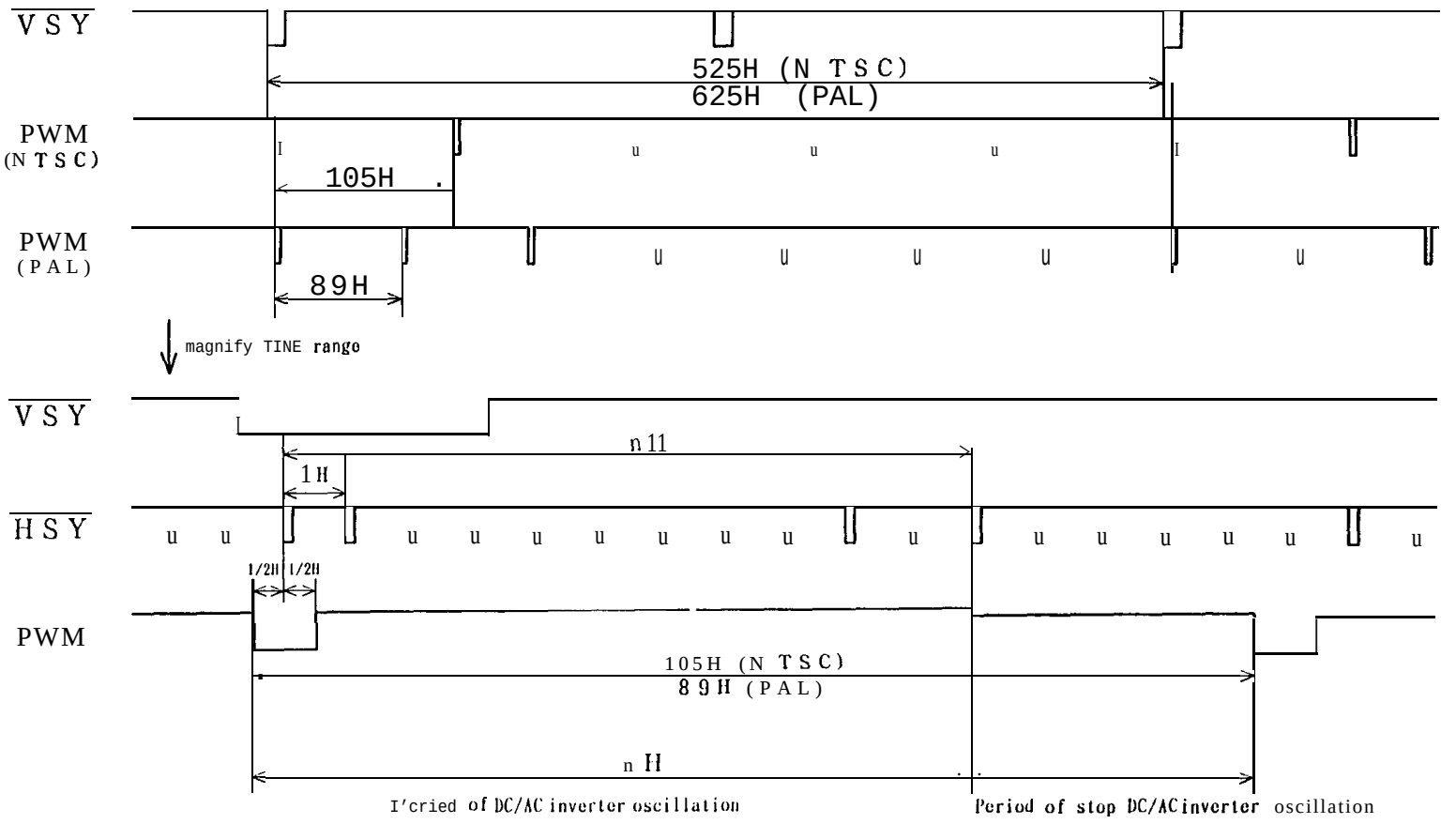


Fig. 5 Adjustment light by PWM signal waveforms